C1 into a low power self refresh mode for the duration of the system level standby/suspend mode. This may be done for example by pulling a memory clock enable line low and other suitable pins to put the memory in a self refresh mode. The synchronous memories are designed to switch into energy savings modes based on the level of the memory clock enable signal. In addition, the memory clocks, engine clocks, register clocks and other clocks are also disabled during suspend mode to save energy.

Please replace the paragraph beginning on page 6, line 1 with the following rewritten paragraph:

C2 In one embodiment, an engine clock source is also coupled through a switching circuit such that it is selectively output to one or more processing engines, such as video overlay engines, video capture engines or any other suitable data processing engine, storage circuits or other suitable circuits. As such, the engine clock provides clock signals to memory requests engines and other general purposes processing engines for example, programmable read write registers. The switching circuit disables the output from the engine clock based on register condition data. register condition data may include, for example, whether a multimedia port has been enabled, whether a video capture processor has been enabled, whether standby mode has been enabled, whether a graphic user interface is active, or any other suitable condition.

Please replace the paragraph beginning at page 6, line 18 with the following rewritten paragraph:

C3 FIG. 2 shows one example of a power consumption reduction circuit 200 having a memory clock source 202 and a memory clock divider circuit 203 operatively coupled to a plurality of memory read latch circuits 206. The plurality of memory read latch circuits 206 receives memory data 208 that is read from memory such as frame buffer memory (not shown). The memory read latch control circuit 204 dynamically activates and deactivates the plurality of memory read latches 208 through a control signal 210 based on detected memory read requests 212. The detected memory read requests 210 based on detected memory read requests 212. The detected memory read requests 212 may be any suitable memory access request from a suitable requestor, such as a graphic user interface engine, video overlay engine or any other suitable memory request engine.

Please replace the paragraph beginning at page 8, line 18 with the following rewritten paragraph:

C4 FIG. 3 illustrates an example of a power consumption reduction circuit 300 employing a memory clock divider circuit 302 that is responsive to memory clock condition data 304, and an engine block circuit 306 responsive to engine clock condition data 308. Examples of engine clock condition data include, for example, data representing whether I2C is enabled or whether a multimedia port is enabled. These may be user defined. Other examples include data representing a host write buffer is not empty, whether video capture engine is enabled, whether an overlay scaler is enable, whether a CUI engine is active and any other suitable condition. As shown in this embodiment, a memory controller 310 may include, if desired, the power consumption reduction circuit 200 to control the memory read latches as previously described. However, it will be recognized that the circuit 302 and 306 may be used each alone or in combination with one another and with the power consumption reduction circuit 200. Also shown in this embodiment is a variable memory clock speed control circuit 312, such as that described in co-pending patent application having attorney docket number 0100.01253, Serial No. 09/130,746, filed on August 7, 1998, entitled "Dynamic Memory Clock Control System and Method", by Lee et al., owned by instant Assignee and hereby incorporated by reference. However, it will be recognized that the variable memory clock circuit may be omitted or that any suitable variable memory clock speed control circuit may be used.

Please replace the paragraph beginning at page 10, line 8 with the following rewritten paragraph:

C5 Such a combination of condition data is shown for AND circuit 322c. In this example, the graphic user interface engine receives the independent clock signal 320c only after GUI active condition data 330 and GUI write data 332 are active. The GUI write condition data 332 indicates that the GUI write buffer is not empty so that the system knows when the GUI engine is finished writing to memory. Other condition data for the memory clock divider circuit 302 includes scaler enable data 334, subpicture "on" data 336 indicating that the subpicture operation has been selected, video capture enable data 338, half frame buffer data 340 and scaler enable data 342. Condition data 338, 340 and 342 are used for a video capture engine so that the

C5 memory clock to the video capture engine will be disabled if none of the video capture related condition data is met.

Please replace the paragraph beginning at page 11, line 1 with the following rewritten paragraph:

C6 Engine clock circuit 306 includes an engine clock signal 360 coming from an engine clock source as known in the art. The engine clock signal is independently and selectively disabled for any suitable engine. As shown, a switching circuit 362 generates an output clock signal 364. Engine clock condition data is used to selectively couple the clock signal to at least one of a video overlay engine, a video capture engine, serial interface (e.g., I2C type) control logic and a multimedia port (MPP), or any other suitable processing engine such that the switching circuit 362 disables the output clock signal 364 based on condition data. by way of illustration, the switching circuit 362 may include an OR circuit 372 and AND circuit 366 and another AND circuit 368. The AND circuit 366 receives the engine clock signal 360 and a suspend/standby command signal 370. The engine clock signal 360 is then passed through the AND gate 366 when the suspend and standby mode is inactive, indicating normal operating mode. The OR gate 372 serves to allow any of the condition data to output the engine clock signal 360 through AND gate 368. In this example, OR gate 372 receives I2C enable data, multimedia port enable data, host write buffer data indicating whether the write buffer is empty, video capture enable data, overlay enable data, GUI engine active enable data, register access data (indicating that registers are being programmed), or any other suitable condition data. as such, an I2C engine 374 or a multimedia port 376 may have the engine clock signal selectively enabled or disabled based on requisite condition data. this facilitates a fine tuning capability from a power consumption perspective to allow both the engine clock and memory clock to be selectively disabled based on user selected conditions or activity based conditions. For example, where the system is employed in a graphic accelerator chip, the memory clock to the video overlay engine may be disabled by accelerator chip, the memory clock to the video overlay engine may be disabled by providing a scaler enable signal as user selected such that the memory clock signal 320d is not sent to the overlay scaler. In addition, an overlay enable signal may also be used as condition data to the engine clock control circuit 306 to prevent the associated registers for the overlay engine to be disabled by effectively disabling the engine clock to the

C6 overlay engine registers. In this way, a host processor and/or graphics processing engines cannot access the requisite registers associated with the video capture or video overlay engine.

IN THE CLAIMS

Please amend Claims 1, 8 and 17-19 to read as follows. In particular, please substitute the below claims for the same claims with like number.

C7

1. (Thrice Amended) A power consumption reduction circuit comprising:

a memory clock source of a graphics controller; and

a memory clock tree circuit of a graphics controller, operatively coupled to the memory clock source, that generates branches of memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines and selectively activates at least some of the plurality of independent clock signals in response to received condition data during an active mode.

C8

8. (Thrice Amended) A power consumption reduction circuit comprising:

a memory clock source of a graphics controller;

a memory clock tree circuit of a graphics controller, operatively coupled to the memory clock source, that generates branches of memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines and selectively activates at least some of the plurality of independent clock signals in response to received condition data;

an engine clock source operatively coupled to a switching circuit that generates an output engine clock signal that is selectively coupled as a clock signal to each of a plurality of registers associated with at least one of: a video overlay engine, a video capture engine, I2C control logic and a multimedia port, such that the switching circuit disables the output engine clock signal in response to receiving condition data; and

a plurality of memory read latch circuits and a memory read latch control circuit operative to dynamically activate and de-activate the plurality of memory read latches based on detected memory read requests to facilitate memory access activity based power reduction.

C9

17. (Twice Amended) The circuit of Claim 1, wherein the received condition data includes data representing at least one of: whether a primary or secondary display has been

C9

selected, whether a graphic user interface engine is active, whether a video overlay scaler has been enabled, whether subpicture operation has been enabled, and whether video capture operations have been enabled.

18. (Twice Amended) The circuit of Claim 8, wherein the received condition data includes data representing at least one of: whether a primary or secondary display has been selected, whether a graphic user interface engine is active, whether a video overlay scaler has been enabled, whether subpicture operation has been enabled, and whether video capture operations have been enabled.

19. (Twice Amended) The method of Claim 13, wherein the received condition data includes data representing at least one of: whether a primary or secondary display has been selected, whether a graphic user interface engine is active, whether a video overlay scaler has been enabled, whether subpicture operation has been enabled, and whether video capture operations have been enabled.